

Philips Development System Mother Board for 8xC51MX (Memory eXtended) Microcontrollers

PDS51E

FEATURES

- Supports the New Philips 51Mx (Memory eXtended) family of microcontrollers
- Universal motherboard with device-specific daughterboard and footprint-specific header
- Real-time transparent in-circuit emulation to full rated device speed over full device voltage range
- 256k bytes memory for user program code
- Real-time trace (128k frames x 64 bits) including 12 user input channels
- Multiple breakpoint sources
- Trigger output for synchronising external equipment
- Programmable clock and supply voltage
- Fast USB interface to host PC
- Sophisticated Windows-based debugging environment
- Fully field-upgradeable logic and firmware
- Free updates and product support at www.pds51.com

DESCRIPTION

The PDS51E motherboard is the basis for an advanced 3rd-generation fully-featured board-level in-circuit emulation system for Philips 8xC51-family microcontrollers.

It allows complete control over execution of a user's program, and access to all internal registers and memory spaces of the target microcontroller, without consuming any resources or introducing wait-states or other non-standard behaviour.

This means that the microcontroller in the user's target system can be replaced with the PDS51E motherboard fitted with an appropriate target-specific daughterboard, enabling the system to be easily run and examined in order to perform program debugging and optimisation.

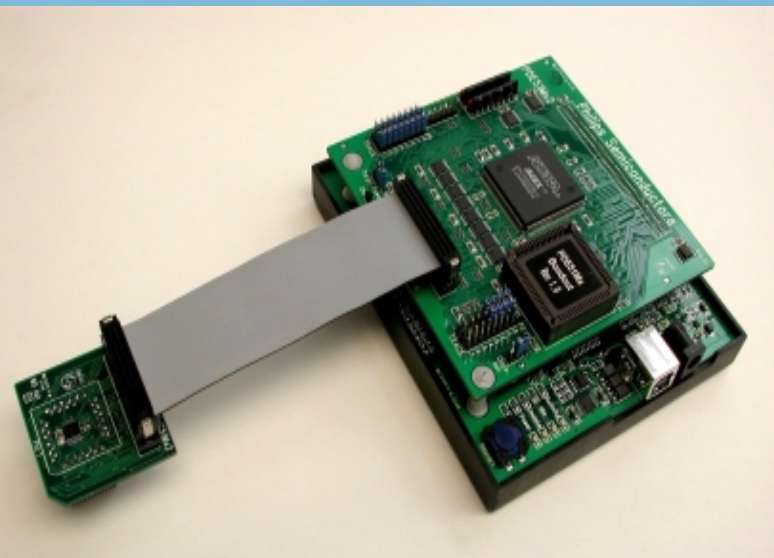
A complete emulation system comprises two interconnected board-level modules - the PDS51E universal motherboard and a bondout-based target-specific daughterboard. A separate footprint adaptor connected via a flat ribbon cable provides flexible support for various device packaging options.

The PDS51E is supplied with sufficient memory to enable emulation of 256k bytes of directly-addressable program memory, and recording of a trace history comprising 128k frames of 64-bit wide data. Information is recorded in the trace buffer in real time for every machine cycle and comprises address, status, operand and SFR data, and 12 channels from external inputs. An additional 256k bytes of memory provides breakpoints and ancillary control and output functions.

Versatility is greatly enhanced by the inclusion of a PLL-based programmable clock source, and a programmable power supply which allows emulation over the full range of clock rates and supply voltages supported by the target microcontroller. An isolated universal mains power supply is included in the box and eliminates potential problems with earth loops. A trigger output permits synchronisation of an external oscilloscope or logic analyser to any selection of fetch addresses in the 256k program memory space, and an external input can be qualified by any selection of addresses in order to break execution. A continuous clock source is provided to hold off any external watchdog.

The PDS51E interfaces to a host PC via a USB interface cable that provides ease of installation and fast communication. The host PC runs a sophisticated Windows-based debugging environment that supports all popular code generation tools from 3rd-party vendors. The debugger runs on all versions of Windows that support USB.

The design of the PDS51E system is uniquely "soft" in that all firmware and programmable logic on both the motherboard and daughterboard can be field upgraded in order to improve performance or add new features. Upgrades are available free of charge from the Web and the debugger can be configured to automatically check and advise of new updates and download them as desired.



A compatible daughterboard and footprint adaptor is required for a complete emulation system

The PDS51E motherboard may be ordered from Philips Semiconductors or their distributors under part number PDS51E SD. For Internet sales and support visit www.pds51.com.

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SPECIFICATIONS

- **Architecture**
 - Universal motherboard
 - Target device specific daughterboard
 - Target footprint specific header
 - Fast USB interface to host PC (2m USB cable included)
 - Windows-based debugger
 - Fully field-upgradeable logic and firmware
- **Emulation**
 - Transparent - no stolen resources no wait states
 - Real-time to beyond rated target device speed
 - 256k bytes of memory for user programs
- **Trace Memory**
 - 128k frames deep, 64 bits wide
 - One frame recorded per machine cycle
 - 23-bit program address
 - cycle status (instruction fetch, operand fetch, interrupt, idle, etc.)
 - 8-bit source, destination, SFR data
 - 12 user input signal channels
- **Breakpoints**
 - 256k on program fetch addresses
 - 256k on program fetch address AND external user input
 - Break on full trace buffer (128k frames)
 - Break after N instructions (N = 1..2³²)
 - Break on fetch outside valid program address range
 - Break on stack address range violation
 - Break on user request
- **Trigger Output**
 - For synchronising external test equipment
 - 256k on program fetch addresses
 - 4 modes at each address (none, pulse-invert, set, clear)
- **Other Interface Signals**
 - Watchdog output - to hold off external watchdog resets when execution halted
- **Processor Clock**
 - PLL synthesiser with quartz crystal reference
 - programmable from 25kHz to 100MHz at better than 0.1% accuracy for any frequency (actual usable range limited to that of the target bondout device)
 - Selectable optimisation to minimize jitter or maximize frequency accuracy
- **Processor and System Power Supply**
 - Voltage programmable from 0 to 5.5V in 25mV steps (actual usable range limited to that of the target bondout device)
 - Supplied with fully-isolated universal mains power supply (input 90-260VAC @ 40-60Hz, output 5.0VDC @ 1.5A)
- **Indicators**
 - System power
 - USB communications/system activity
 - Emulation (execution)
 - Idle mode

WINDOWS DEBUGGING ENVIRONMENT

- **Requirements**
 - Pentium PC with 128M RAM, USB Port, Windows 95 (SP2), 98, ME, 2K or XP
- **Features**
 - Project-based for rapid swapping between projects.
 - Source-level debugging with extended OMF files.
 - Rich feature set with Borland-compatible debugging control keys.
- **Resizable Panes**
 - Any number of panes displaying any of:
 - C or Assembly-language Source
 - Disassembly
 - Mixed Source/Disassembly
 - Internal RAM
 - External RAM
 - Stack
 - Trace
 - Watch (can display and modify any SFR or variable in any of the supported display formats (hex, unsigned, signed, octal, ASCII character, binary, float, Pascal string, or C string).
- **Emulation Controls**
 - Reset target
 - Set execution point
 - Run
 - Stop
 - Run to Cursor
 - Step
 - Step N times
 - Step into procedure/function
 - Step over procedure/function
 - Leave (run until procedure/function exits)
 - Follow (reposition view at target of a flow-change instruction)
 - Clear trace buffer
 - Run until trace buffer full or filled again
- **Trace Display**
 - 128k frames
 - Address
 - Operand
 - SFR read data
 - SFR write data
 - Status
 - 12 User inputs
 - Disassembly of instruction
 - Analysis of data transfer
- **On-line Help**
 - Context-sensitive
 - Full 8051MX instruction reference
- **Environmental**
 - Low-cost board-level product in plastic tray base
 - Complies with European CE specifications
- **Size**
 - Motherboard and Daughterboard combined (excluding footprint adapter and header)
 - 130mm x 110mm x 40mm (L x W x H)

Disclaimer: Specifications subject to change at any time without prior notice