

■ Hardware description

A PDE5IMX daughterboard and a PDS5IE universal motherboard combine to form a very affordable yet powerful fully-featured transparent real-time emulation system to support development of products based on the Philips 5IMX (memory extended) family of 8xC5I derived microcontrollers.

The PDE5IMX daughterboard is based on a special version of the standard 8xC5IMX microcontroller with additional signals required to support emulation bonded out. It also employs reprogrammable logic to allow field upgrades of the system logic in order to enhance performance or provide additional features.

■ Daughterboard installation and removal

Please ensure that the power supply and USB cables are disconnected from the PDS5IE motherboard. Carefully align the 100-pin connector on the daughterboard with the mating connector on the PDS5IE motherboard. The plastic spacers should also align with the holes near the front edge of the daughterboard. When you are satisfied with the alignment of the connectors, press them firmly together until they are fully mated. Similarly mate the spacers. Take care not to flex the boards.

Attach the footprint adaptor header to the daughterboard using the 50-way flat cable assembly provided.

Connect the power supply and USB cables to the motherboard.

To remove a daughterboard, disconnect the power supply and USB cables, remove the header, disengage both plastic spacers (by pressing down on them with the thumb while lifting the corner of the daughterboard with the fingers), and carefully disengage the mated connectors taking care to keep them as parallel as possible. Take care not to flex the boards.

■ Footprint Adapters

Each daughterboard is supplied with an appropriate standard target footprint adaptor and header assembly. For the PDE5IMX daughterboard the footprint adaptor is a plug compatible with a standard 44-pin PLCC socket. As additional device packages are introduced, suitable footprint adaptors for these will become available at additional cost.

■ Bondout Clock

The bondout clock for the PDE5IMX is generated by a crystal-locked PLL synthesiser on the PDS5IE motherboard. The frequency may be set from the debugging environment and can potentially be programmed to any frequency in the range 25kHz to 100MHz (upper bound subject to actual limitations of the bondout device) with an accuracy of 0.1%.

Note that the 8xC5IMX is based on a 6-clock core and hence executes at twice the speed of a standard 8xC5I 12-clock microcontroller at the same clock frequency.

With a 5V supply, emulation can typically be achieved at clock frequencies in excess of 30MHz, corresponding to an equivalent clock frequency in excess of 60MHz for a standard 8xC5I device.

A jumper allows the clock to optionally be fed to the XTAL2 pin on the target footprint connector. It is not possible to source the bondout clock from the target system.

■ Restart Button

The PDS5IE motherboard has a button labelled RESTART which forces a complete reset of the motherboard and daughterboard systems including USB re-enumeration, reloading of all system firmware, and re-configuration of all programmable logic. It should not be confused with the active-high target RESET input (pin 10 on the 44-pin PLCC package) which resets the bondout and forces execution to restart at address 0.

■ Trace Blocks

The PDE5IMX daughterboard provides 12 input channels to allow recording of external digital signals synchronised with traced execution. These signals can either be connected to the target system via external probe leads, or jumpers can be installed on the daughterboard to conveniently trace selected subsets of I/O port pins. Jumpers are installed by default but a set of probe leads is also supplied.

There are two trace-blocks - TR0 on the left and TR1 on the right. Each row in each trace block comprises three pins. The centre pin of each row is the trace input connection and the outer pins are connected to the I/O port pins as per the legend on the PCB.

Trace block TR0 allows jumpers to be installed in all 8 rows in order to trace 8 signals present on ports P0 and/or P2. You cannot however use jumpers to for instance trace both P0.3 and P2.3 simultaneously (although you can do this using probe leads).

Trace block TR1 allows jumpers to be installed in 4 out of the eight rows in order to trace 4 signals present on ports P1 and/or P3. Jumpers cannot be present in corresponding rows of both the upper and lower half of the TR1 trace block since the centre pins of these paired rows are connected together. For instance you can trace P3.0 and P3.7 simultaneously, but not P3.0 and P3.4 (nor P3.0 and P1.4).

All trace inputs have a 1 Megohm pull-up resistor to the bondout supply rail.

■ Inputs and outputs

A 5-pin header on the left edge of the PDE5IMX daughterboard provides four input/output connections and a common ground reference. The function of these is as follows:

- **BP** - a low level present on this input when the fetch address matches any of 256k External Breakpoint settings in the debugging environment will cause execution to break. It is typically used to qualify

breakpoints with the occurrence of a condition in the target system or the output of an external pattern-recognition system (logic analyser etc.)

- **TI** - no function is currently assigned to the input.
 - **ET** - an output intended to be used to provide a trigger stimulus to an oscilloscope or logic analyser. The debugging environment allows up to 256k “trigger points” to be established such that this signal is either unchanged, set high, reset low, or briefly inverted (pulsed) when a fetch is made from the associated address.
 - **WD** - an output providing a continuous square wave intended to be used to hold off an external watchdog in the target system while execution is stopped or when single-stepping. This output signal is also available on the footprint header.
- **Clock Out Jumper**
The XTAL2 clock output signal can optionally be fed out of the footprint adaptor by installing the jumper labelled Clock Out. In order to minimise system noise it is recommended that this jumper only be installed when absolutely necessary. The clock signal is buffered both on the daughterboard and the header and hence is delayed relative to the XTAL2 output of a real microcontroller by about 7ns.

General Notes

- **Bondouts**
Any 85C51MX bondout device in a 68-pin PLCC package may be used in this daughterboard.
- **ALE**
The ALE output can be turned off for reduced system noise in the same manner as in the real microcontroller device (via the AO bit in the AUXR SFR) without adversely affecting emulation. The ALE signal is buffered on the footprint header and hence is delayed relative to the ALE output signal from a real microcontroller by about 5ns.
- **Clock Source**
The clock source for the bondout is always derived from the programmable PLL synthesiser on the system motherboard. Do not attempt to supply a clock from the target.
- **Minimum Operating Frequency**
Real 8x51MX devices are based on a static CMOS core and can hence be run down to 0 Hz. Since the emulator requires the bondout device to be able to execute instructions under all conditions the lowest clock frequency which can be programmed is 25kHz.
- **Maximum Operating Frequency**
The maximum operating frequency for real 8x51MX devices depends on the supply voltage. At any given supply voltage the emulator is guaranteed to operate at the specified maximum clock frequency and will generally operate considerably faster. The debugging environment allows the frequency to be set above the maximum.

- **Operating Voltage Range**

The bondout supply voltage can be programmed anywhere in the range specified for the real 8x51MX device (to a resolution of 25mV), however care should be taken to ensure the programmed clock frequency is then within the device specifications. The debugging environment will not allow the supply voltage to be set outside the specified operating range for the selected target device.

- **General Precautions**

In powering up the emulation and target systems the following sequence should be observed:

1. Connect the 5V DC power supply to the motherboard.
2. Connect the USB cable to the motherboard
3. Apply power to the target system

Power down in the reverse sequence.

Under no circumstances should you attempt to connect/disconnect the emulator and target systems with power applied to either.

All I/O pins on the target connector are either connected directly to the bondout device or to logic which regenerates ports. It is hence important that you do not apply voltages to these pins from low-impedance sources in the target system which exceed the programmed bondout supply voltage by more than about 0.5V. Similar comments apply to the trace inputs and the emulator input/output pins. Failure to observe this precaution may cause permanent damage to the emulator.

All port pins have the same high current sinking capability as the real 8x51MX device. It is hence important that you do not hold port pins high while they are programmed to output 0's. Excess current flowing under these conditions may cause permanent damage to the emulator.

The damage caused by either type of abuse is distinctive and easily diagnosed by our engineers, and the standard warranty specifically excludes any necessary repairs.

- **Warranty**

Our PSD51E+PDS51MX emulation systems are guaranteed for a period of 12 months from the date of sale and will be repaired or replaced at our discretion as appropriate. This guarantee does not cover damage due to excess voltage or currents as detailed under General Precautions and will not apply to units which are physically damaged or modified in any way.

- **Ordering**

The PDE51MX daughter board may be ordered from Philips Semiconductors or via their distributors under part number PDE51MX SD. For Internet sales and support visit www.pds51.com

Disclaimer: Specifications subject to change at any time without prior notice.