

■ Hardware description

The combination of your *PDS51-Mk2* mother board and your *PDB591* daughter board produce a powerful, fully featured, real time development system for ROMless, Masked ROM, and EPROM versions of 8xC551, 553, and 591 Philips microcontrollers.

■ Installation

The *PDB591* daughter board is the first of a series of 6 clock microcontroller daughter boards with a PLL Bondout oscillator and is for use only on a *PDS51-Mk2* motherboard.

Prior to installing the *PDB591* daughter board, ensure that all power sources are removed from the existing system and that appropriate anti-static precautions are being practised.

The daughter board is installed with the footprint adapter plug facing towards the outside edge of the system with the RESET push-button closest to the power input socket. The connections from the *daughter board* to the *PDS51-Mk2* are fitted with polarising, blanking plugs to assist in correct orientation.

■ Footprint adapters

Each daughter board is supplied with a header cable and plug to simulate the footprint of the standard microcontroller under emulation.

The *PDB591* is supplied with a 44pin PLCC header. Contact your distributor for other footprint adapters for different package types.

■ Bondout Oscillator

The *PDB591* daughter board uses an on-board PLL Crystal oscillator where the Bondout operating frequency is changed by the IDE software. (see IDE Help for more information).

The frequency range is guaranteed through the range 1.5 to 12 MHz when used on a *PDS51-Mk2* motherboard. This is equivalent to 3 to 24 MHz of a 12 clock conventional 8xC51 device.

It is not possible to utilise the external clock on your target board with this daughter board.

If the target system requires that the Xtal2 output from the microcontroller be available, then jumper *J1* should be in place to feed this signal back to the footprint adapter.

■ Reset

The RESET push-button on the daughter board resets the *PDS51-Mk2* system. The effect is the same as when the system was initially powered up except that the users code memory remains intact and the internal contents of the microcontroller are preserved.

A successful reset is indicated with a sign on message of the following format:

**PDS51 S/W 2.02 PCB 2.02 DB591 1.0 PML 11
654321 Bondout 8xC591**

This line of information gives the current software

version number, the mother and daughter board revision numbers, the PML hardware revision and the emulation configuration. Any correspondence regarding this product should quote this line of information.

■ Trace Block

The middle row of the 3x header pins on the left hand side of the daughter board provides the 12 traceable inputs to the *PDS51-Mk2*. This row of pins may be connected to logic signals on the target system through flying leads or jumpered to the left (port 1.x and port 0.x) or the right (port 2.x and port 3.x) set of pins, to trace port pin status directly. As supplied, the trace is normally jumpered for P2.0 - P2.7 and P3.2 - P3.5. The bottom three pins of the bottom trace block are all connected to GND.

If the jumper blocks are removed, it is possible to plug onto the centre pins of the trace block with the supplied coloured trace lead sets and to clip onto various points on your target board to trace the operation of these points on the IDE.

The trace pins are connected directly to high impedance CMOS inputs. These inputs are protected by clamp diodes to the +5V supply in the *PDS51-Mk2*. The input levels are TTL level compatible and 5.0 Volts should not be exceeded.

■ DB Extension

The daughter board extension header adds four further functions to the *PDS51-Mk2*.

● \overline{FT}

The **FORCE TRACE** input allows the user to selectively trace execution with reference to a hardware event. All traceable information is unconditionally written to the trace buffer while this pin is pulled low.

● \overline{BP}

A low level on the External **BREAKPOINT** pin will cause the *PDS51-Mk2* to break execution when the address set in the IDE (Setting:External Breakpoint) is executed.

● ET

The **EXTERNAL TRIGGER** pin is used to produce an output which may be used to synchronise external test equipment to the code being executed. This output will be high while executing from the address specified by the IDE (Setting:External trigger) and is low otherwise.

● EM

The **EMULATION** output goes low whenever the code is being executed. The EMULATION LED is also connected to this output to provide visual indication.

The \overline{FT} and \overline{BP} inputs are active low, TTL inputs, terminated with a 47k pullup resistor and diode clamped to the +5V supply of the *PDS51-Mk2*. ET and EM are 5V CMOS outputs.

■ A/D Reference voltage selection

The **8xC591** A/D ports also have a AVref voltage pin and a AVss ground pin.

The daughter board has 2 additional sets of jumper blocks (see diagram).

The AVref+ three way jumper block is used to select either AVref+ from external (down the connecting cable to the target board) or from the +5Volts of the daughter board.

The AVss pin is always connected to the target board down the connecting cable. When the AVss jumper is jumpered to the ground pin, it will also connect the AVss lead to the daughter board ground.

General Notes

■ Port 0 and 2 output levels

As the **PDS51** development system uses emulation microcontrollers with a process called Metalink Hooks, some of the port pins (usually ports 0 and 2) are regenerated by the emulator. This will mean that these port pins do not have exactly the same quasi I/O performance as the genuine microcontroller.

With P2 the two clock additional pullup (see microcontroller quasi I/O data sheets) is not present on the **PDS51** daughter boards. The regenerated port pins are supplied from CMOS open collector ports (with 50ns high drive) pulled high by typically 47k resistors. In some cases, particularly with larger capacity loads, it may be necessary to temporarily add pullup resistors (1k to 4k7) to your target board if there is any trouble obtaining a good fast high level signal when emulating.

■ Watchdog timer

The watchdog timer is not supported on this daughter board.

■ ALE

Some new Philips microcontrollers allow ALE to be turned off to reduce interference radiation. It is NOT possible to turn the ALE signal off on our daughter boards as ALE is fundamental to the operation of the emulator.

■ Minimum Operating Frequency

Some new Philips microcontrollers have static cores allowing operation down to 0 Hz i.e. stopped or single step mode. This is not possible with the **PDS51/PDB591** combination and a minimum frequency of greater than 1.5 MHz is required.

■ Operating Voltage

The **PDS51** system operates only at 5 Volts $\pm 10\%$.

■ General Warning

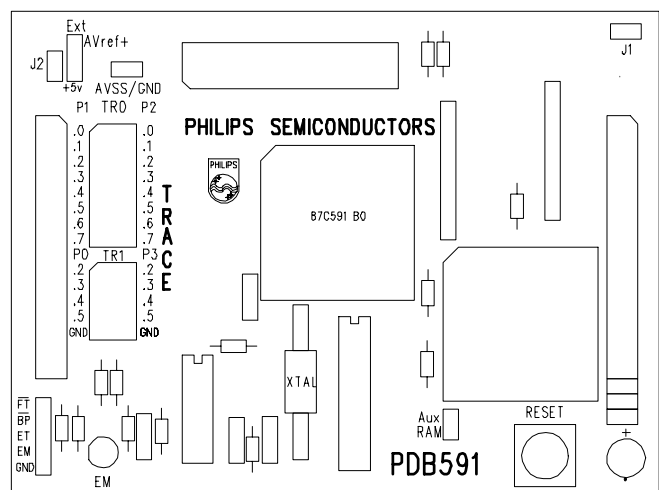
All port pins are either connected directly to the emulation microcontroller or to the regenerated port device. It is therefore very important that voltages levels over 5 volts $\pm 10\%$ are NOT applied to these pins or damage will occur.

It is also very important that external pins on the target board are not held hard high or hard grounded when the microcontroller has been programmed to output the opposite potential on the same pins. Excessive currents can flow and damage to the emulation microcontroller port structure will occur.

It is not possible to emulate push-pull port pin operation on the regenerated ports of the **PDS51-Mk2/PDB591** combination.

All daughter boards are supplied using the most powerful "super set" of the particular series of emulation microcontrollers. It is therefore very important to remember not to use those features that MAY be available on these particular devices that will not be available on your final end use microcontroller.

This included such things as extra internal RAM, Aux RAM, larger ROM, dual data pointers etc. Use only features as shown in the data sheets for your chosen microcontroller.



Daughter Board Jumpers

Jumper	Default	Function
J1	off	Xtal2 connection to footprint
J2	open	Factory test only
AVss	on	AVss output pin connected to daughter board ground
AVref+	+5V	AVref+ supply from daughter board +5Volts
Aux RAM	on	Aux RAM enabled

For daughter board help, the latest up to date information, or any application note for this daughter board, please check the help or document files on the latest copy of your IDE software.